GUEST EDITORIAL

Point-to-point architectures are undeniably en route, yet there's still a lot of fuel left in the tanks of bus architectures

By John Sotir

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Deep in the trenches of the communications equipment and semiconductor business an architectural debate has been brewing for the past few years. The debate centers on the relative merits of traditional bus architectures versus the newer, point-to-point switch fabric architectures. A key question being debated is when and how fast the much more widely deployed and established bus architectures will get replaced by point-to-point architectures.

Point-to-point architectures are undoubtedly going to be used widely in the future. Yet there is a lot of fuel left in the tanks of bus architectures, probably more than any of us might have believed just a few years ago. The reasons for this are numerous. One major reason is the recent industry downturn that has dramatically reduced capital investment by communications equipment and service providers.

Indeed, such equipment manufacturers in increasing numbers are shifting back to established and stable approaches attainable using bus technology. And they are going to continue to use them for the next few years at least – longer than was expected before the downturn. The downturn has focused attention on economic improvements and functional expansion on existing equipment systems.

Bus architectures offer several key benefits when used in their typical equipment applications such as computer telephony integrated solutions, multi-service access platforms, media (VoIP) gateways, telephony servers, and wireless base station controllers. Such benefits include low costs, simplicity of implementation, low power consumption, and low component count. Bus architectures are also widely embraced by the industry and tend to be, for now, more interoperable than point-to-point switched architectures.

Two well-defined and well-established technologies that use buses, Time Division Multiplexing (TDM) and Asynchronous Transfer Mode (ATM), have proven that they work in real-world field applications. They are standards-based and allow for incremental and relatively inexpensive equipment upgrades. These technologies exist today and have been deployed in various systems for years.

Equipment manufacturers generally are comfortable using these TDM and ATM technologies because they have been doing so for several years. These are not technologies that require a manufacturer to invest lots of time and money getting up to speed on what they are and how they are to be used. These bus technologies are mature. Devices supporting these architectures have a low price-to-performance ratio.

While acknowledging these numerous merits of bus technologies, there is no question that point-to-point architectures are becoming more attractive and are bound to be used widely in the future. They will be used in many of the same types of equipment as bus architectures, such as voice over Internet Protocol gateways, digital subscriber line access multiplexers, media gateways, and multi-service access systems. Compared with bus architectures, point-to-point architectures typically provide higher bandwidth due to faster data transmission.

For high-end communications equipment applications, architectural designs will undoubtedly be migrating to point-to-point mainly because of the relatively high capacity and high speeds it enables. However, for incremental or near-term equipment designs – and essentially most types of equipment systems not requiring high bandwidth, bus capacities are still applicable and attractive. For such lower-end equipment, data capacities using reliable bus architectures are still sufficient and can be implemented at a lower cost.

Still, critics of bus architectures contend that point-to-point architectures are inherently more reliable. This capability is a major and compelling argument in their favor. Critics point out that if a bus goes down, it is more likely than a point-to-point system to shut down the entire system or whatever technologies were touching that bus. Using point-to-point architectures, one such isolated failure only causes the location of that failure to be affected and not the whole system. Actually, bus architectures are also incredibly reliable when analyzed from the point of view of how often such buses really shut down an entire system.

The issue boils down to this: If you need capacity, you need capacity, and point-to-point solutions are the way to go. If you don't have to go with a new high-capacity, high-end design, bus architectures are already well-defined and a viable low cost option. There are existing semiconductor solutions and equipment solutions built for bus architectures that make it easier to quickly design equipment. Using a new point-to-point architecture requires extensive development effort to verify performance. Such effort increases material and device costs.

This longer life expectancy of bus architectures stems in part from the recent economic and communications industry slowdown. The decrease in capital spending by communications equipment manufacturers during the past year and a half has slowed demand for next-generation, point-to-point technologies. Equipment manufacturers have decided to hold off on spending as much money as had been previously planned from a few years ago on higher capacity and faster equipment. They are doing this to control expenses and synchronize the availability of such higher-end, point-to-point products to coincide with the rollout of new, high bandwidth services.

Rather than taking big jumps with higher-capacity, point-to-point technologies, manufacturers are making more incremental modifications to their current hardware. Their plans devised during the past few years to make core switching routers, for example, have been delayed because of declining demand and rising equipment inventories. They are discovering that developing such equipment consumes more time valuable resources they can no longer afford to lose. Such manufacturers are relying on technologies they already know how to make.

From a communications device design and manufacturing point of view, Agere Systems continues to focus on designing and manufacturing integrated system devices that can work in both bus and point-to-point architectural configurations. Our existing product portfolio provides device solutions that support reduced cost, size, and power consumption, which addresses the capital expenditure-constrained environment of today, and the increasingly complex, higher-performance needs of tomorrow. Looking to the future, Agere's new product portfolio of devices focuses on implementing high capacity, point-to-point technologies. These new devices satisfy the leaps in performance required by next generation product and system designs.

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Agere Systems continues to listen to its customers and monitor carefully their investment decisions. Many have concluded that it makes sense to keep riding those buses for awhile longer. There's still lots of fuel left in the tanks of these buses. Bet on them taking where you want to go for longer than you might have been planning. And continue to watch, prepare, and react carefully to this accelerating bus and point-to-point race being driven around the communications equipment industry.

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Devices available today

In the semiconductor device arena, there are established and available semiconductor devices built to perform TDM and ATM functions. Agere Systems designs and manufactures integrated communications components that support TDM and ATM technologies. The company's Ambassador® series provide time-slot switches incorporating an interface for the H.100/H.110 TDM buses. One of Agere's Ambassador family of devices, the T8110, is a flexible backplane interface time slot interchange that supports switching of time slot data and packet payloads between a local Peripheral Component Interconnect bus and the H.100/H.110 buses. This device is intended to work with a coprocessor to provide header, framer, and checksum generation functions. Because this chip operates purely on payloads, multiple protocols such as ATM and Internet Protocol can be supported simultaneously. The T8110 switches TDM voice traffic between a local to PCI input/output bus and an H.100/H.110 bus to manage TDM traffic.

Another Agere chip, the CelXprex' T8207 ATM switch and backplane interconnect device, integrates all the required functions to transport ATM cells across bussed backplane architectures with high-speed cell traffic exceeding 1.5 GBits/sec, to a maximum of 32 destinations. The device manages multiple service categories and monitors performance.

