



# Measuring the actual performance characteristics of AdvancedTCA backplanes with signal integrity analysis

By Mahamud Khandokar

**W**hen a high-speed product specification is relatively new, there is often little information on the actual performance characteristics of the products as opposed to the theoretical performance given as it is being developed. Perhaps there were simulation studies that provided a basis for the hypothesized performance, as was done for AdvancedTCA. But different companies have different design practices and capabilities. How do we know if a specific vendor's product performs adequately? Particularly with the high speeds of the signals, how do we know if the signal integrity truly holds up across the backplane design? In this article Mahamud will show how the true performance characteristics of an AdvancedTCA backplane can be studied through signal integrity engineering, along with several examples of the measurements.

## Signal integrity engineering

Faster PCB designs are by nature more sophisticated and delicate. At higher clock speeds, the PCB demands cleaner signal transmission without compromising the stability of the system. This is where signal integrity engineering comes into play. Simply put, signal integrity studies the design of high-speed circuits that

can accommodate cleaner signals passing through them. Cleaner signals, in turn, enable engineers to identify and minimize sources of distortion in data transmission, which could otherwise disrupt timing of the digital logic. Signal integrity issues such as reflections, crosstalk, frequency dependent transmission line loss, and dispersion can significantly lead to poorer system performance propagating through the interconnect. These signal integrity issues arise from such elements as via, power/ground coupling, and RLC effects in signal lines. With 3.125 Gbps to 6.250 Gbps signal speeds across the backplane and beyond, an AdvancedTCA backplane is very susceptible to these types of issues.

To ensure customers the optimum performance, backplane simulation/characterization studies can be performed. In this article, we will focus on the characterization of Bustronic's 5-slot Mesh AdvancedTCA backplane. The 5-slot AdvancedTCA backplane was a 3x Mesh in an 18-layer controlled impedance edge-coupled stripline design. We worked with NESAs and Teraspeed on the development of a new AdvancedTCA backplane Signal Integrity (SI) test card. The test card is used to accurately measure the impedance, transmission, channel skew, eye-diagram, and channel crosstalk charac-

teristics of an AdvancedTCA backplane. This SI test card was designed specifically to meet the testing requirements set forth in the PICMG 3.0, AdvancedTCA specification.

AdvancedTCA calls out specific requirements for several parameters of signal integrity, shown in Table 1.

The following studies will show the backplane's performance relative to the specification's requirements.

## Fabric impedance

The first measurement we will discuss on the 5-slot AdvancedTCA backplane is the fabric impedance. (See Figure 1). The characteristic impedance of the transmission line is defined by the ratio of the voltage and current at any point as a test pulse travels down a pair of differential backplane traces.<sup>1</sup> Impedance mismatches (due to vias and connectors) and variations can cause reflections, which degrade the signal quality.

Time Domain Reflectometry (TDR) produces a positive-going incident wave that is applied to the Device Under Test (DUT). The step-pulse travels down the DUT at the velocity of propagation of the line. If the load impedance is equal to the

Differential impedance of the backplane and probe board serial links for base and fabric interfaces	100 Ohm $\pm$ 10%
Differential impedance of the backplane serial links for the clock interfaces on the backplane	130 Ohm $\pm$ 10%
Fabric interface transmit and receive pairs within a channel	Matched delay of better than 17ps each
Worst case trace insertion loss	Follow the "Insertion loss limits for PICMG 3.0"
Edge couple backplane single strip line for FR4 di-electric, near-end coupling coefficient	<0.2%
Fabric interface transmit and receive pairs within a channel	Matched delay of better than 17ps each

Table 1

characteristic impedance of the line, no wave is reflected, and all that will be seen on the oscilloscope is the incident voltage step recorded as the wave passes the point on the line monitored by the oscilloscope. At every impedance discontinuity that the signal encounters, part of the incident wave is reflected. The reflected voltage wave will appear on the oscilloscope.<sup>2</sup> The resulting waveform is like a roadmap of the impedance variations across the trace.

Only the worst case connection paths were tested. For our measurements, we used a wide-band oscilloscope with 18 GHz measuring bandwidth, high-quality cables, termination resistors, and Iconnect analysis software from TDA systems. Testing only the worse case connection paths meant that the longest net length traces were tested. The differential impedance of the backplane and board serial links for base and Fabric interfaces should be 100 Ohm  $\pm 10\%$ . The measured average value of differential trace line is 107 Ohm. Figure 1 proves even the worst case scenario performed within the required range. Figure 2 shows the test set up.

### Clock impedance

There are six synchronization clock buses in the architecture. The six buses are divided into three groups of two differential pairs each. Each clock bus is implemented as a differential pair that connects to all slots through pins in the Zone 2 connectors. The buses are fully symmetric so that receivers and transmitters (bus drivers) can be located in any slot. The first pair of clock buses (CLK1A and CLK1B) is dedicated to redundant 8 kHz system clock signals. This frequency is the fundamental frequency used for all digital telephony transmission systems. The CLK1A $\pm$  is tested. CLK1A $\pm$  net is tested. The differential impedance of the backplane serial links for the clock interfaces on the backplane should be 130 Ohm  $\pm 10\%$ . The measured average value of clock trace line is 124 Ohm. Again, the results were well within the limits.

### S-parameter

Scattering parameters can capture the reflection and transmission from junctions in backplanes. The ratio of the reflected power to the incident power is the return loss, and the ratio of the transmitted power to the incident power is the insertion loss. These values are derived for defined incremental frequency steps over a range of frequencies that covers the design requirements for the backplane.

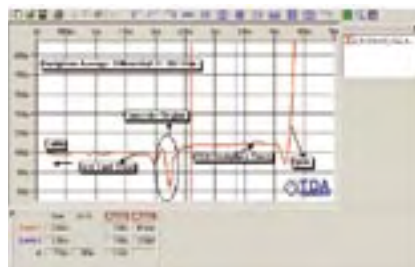


Figure 1: Layer 09\_Slot01\_P22\_AB7 impedance waveform



Figure 3a: Layer09\_Sig04\_AB7\_S21 waveform

For AdvancedTCA this was the range from 0 GHz to 5 GHz.

The results, as shown in Figures 3a and 3b, reveal that both the insertion and return loss on the 5-slot AdvancedTCA backplane under test do not violate the insertion loss and return limits for PICMG 3.0.

### Crosstalk

Crosstalk refers to undesired signals induced on traces or paths due to other nearby signals. Near-end (backward/reversed) crosstalk is defined as the crosstalk seen on the victim line at the end closest to the driver (aggressor). Far-end (forward) crosstalk refers to the crosstalk observed on the victim line farthest away from the aggressor.<sup>1</sup> To achieve accurate

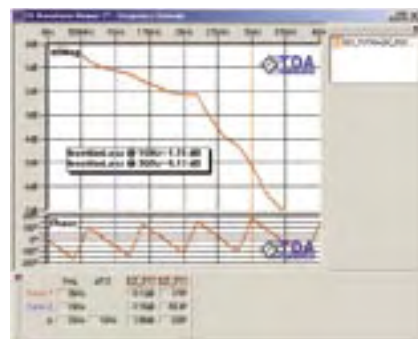


Figure 3b: Layer11\_Sig04\_AB8\_S1 waveform

results, we used high-quality cables, termination resistors, and adapters with our PCB under test. Figure 4 shows the result for Far-End Crosstalk (FEXT).

From the FEXT graph, The aggressor amplitude is 200mV, and the crosstalk in the connector area and backplane trace area are in microvolt range (which is negligible). From our next measurement, the aggressor amplitude is 200mV, and the crosstalk in the connector area is 4mV (only 2%).

### Eye diagram

An eye diagram takes the results of a simulation driven by a long, multi-cycle bisequence, superimposes each bit period

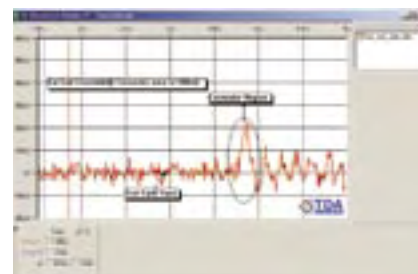
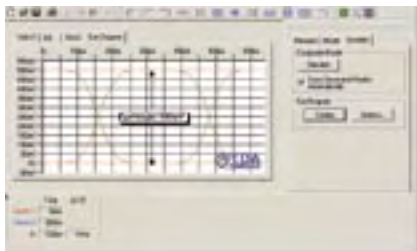


Figure 4: Layer11\_Sig05\_FEXT waveform



Figure 2: Test set up

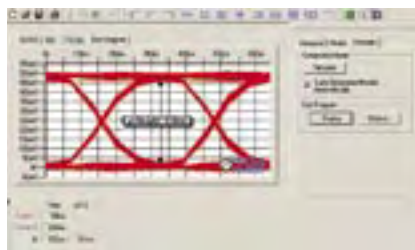
over the top of all others, like a time exposure photograph, and presents waveforms that have open areas shaped something like a human eye. The larger the eye opening, the better the results. The most common type of stimulus used in eye-diagram generation is the *PRBS* or *Pseudo Random Bit Sequence*.<sup>3</sup> From the result (see Figures 5a and 5b), we can see that the trace on Layer 9, which is routed on Slot 1 to Slot 5, still has a more than adequate eye opening (86%) at a PRBS  $2^{10}-1$  of 3.125 Gbps.



**Figure 5a: 5A 3.125 Gbps reference, eye height: 500mV**

#### Performance assured

We were able to show that the 5-slot AdvancedTCA backplane performance was well within the specified requirements, even taking the worst case scenarios. The TDR signal that we used for our measurements has a 35 ps rise time, which is quite fast compared to real-life devices.



**Figure 5b: Slot 1 to Slot 5, eye height: 430mV**

The signal distortion due to inductive and capacitive discontinuities will be smaller at a low rise time signal.

Simulation and characterization capabilities will be increasingly important as we continue to move to higher-speed switch fabric technologies. Bustronic will continue to publish various SI studies, including a study on pre-design simulation of an AdvancedTCA backplane

*Mahamud (Misty) Khandokar is a Signal Integrity Engineer for Bustronic. Misty has several years of experience in characterizing printed circuit boards and backplane interconnects of 1–10 Gbps. Continuing the development of Bustronic’s signal integrity laboratory, she has expanded the company’s program of simulation, backplane characterization, and model creation.*

For more information on this or other SI studies, contact Mahamud at:

**Bustronic, an Elma Company**  
44350 Grimmer Blvd.  
Fremont, CA 94538  
Tel: 510-490-7388 • Fax: 510-490-1853  
E-mail: mkhandokar@bustronic.com  
Website: www.bustronic.com

#### References:

- [1] Stephen H. Hall, Garrett W. Hall, James A. McCall, “High-Speed Digital System Design.”
- [2] “Time Domain Reflectometry Theory” Agilent Application Note 1304-2.
- [3] “3.125 Gbps with your Hair on Fire Simulation-Based Signal-Integrity Analysis of Digital Interconnects at Multi-Gigabit Speeds” by Bill Hargin, High-Speed Systems Design, Mentor Graphics Corporation.