Channel characteristics challenge backplane interoperability

By Stuart Jamieson

Serial backplanes in telecommunications systems aim for high speed with room for growth. As systems began using 10 Gbps links, however, issues arose that affected backplane communications among cards from different manufacturers. Stuart points out that the industry must define key backplane channel characteristics so that designs based on open standards maintain interoperability as backplane speeds move to 40 Gbps and beyond.

Increasing demand for service and multimedia features is stimulating a growing need for speed in telecommunications equipment. While some applications, such as PBX systems, can be addressed with the gigabit backplane technologies currently available, others are running out of headroom. Routers may soon need 10 Gbps and higher speed backplanes to keep up with network demand. Many such applications can justify the expense of moving to higher performance if it becomes available.

Currently, telecom system designs offer backplanes that can handle interconnections running as fast as 3.125 Gbps raw data throughput per lane (with around a maximum data rate capability of 5-6.25 Gbps per lane). The AdvancedTCA standard, for instance, uses Ethernet's XAUI interface. AdvancedTCA achieves a 10 Gbps net data rate by running four serial lanes for each interconnection, with each lane's SERrializer/DESerializer (SERDES) operating at 3.125 Gbps raw data (2.5 Gbs net).

As demand forces systems to move beyond these rates, however, new technologies will be needed. One proposal calls for the use of XAUI+, or double XAUI, which increases lane SERDES rates to 6.25 Gbps per lane and hence the throughput to 20 Gbps. Another proposal is to use IEEE 802.3ap, known as 10GBASE-KR, which runs a single SERDES lane at 12.5 Gbps raw data rate (10.3 Gbps net). But these are only short-term answers. To address future demands organizations such as the Institute of Electrical and Electronic Engineers Standards Association (IEEE-SA) are developing specifications for Ethernet speeds of 40 Gbps to 100 Gbps, which will be applied to backplane interconnect.

Such high clock rates, however, will pose significant design challenges for developers. One of the first challenges that will need resolution is the design and layout of the backplane and other PCBs. Common design practice today readily handles board clock rates of around 10 Gbps. Well established design rules are in place, and board layout tools such as autorouters can automatically handle board designs for speeds in the 10 Gbps range. Designers may use specialized board material, create additional ground planes, and perform similar tasks in order to ensure proper board operation at the higher end, but even speeds to 5 GHz are within current design tool capabilities.

Design gets trickier

Above 5 GHz, however, board design gets more involved because feature dimensions become significant when compared to the signal's wavelengths. Variations in board thickness can affect signal propagation. Corners where traces change direction and small spurs along edges of poorly etched traces can act as antennae for the higher frequencies in digital signals. As can be seen in Figure 1, sharp corners and minor flaws that are inconsequential at lower frequencies have the potential to become troublesome antennae at future high speeds. This can result in the trace radiating away the signal's high frequency energy, increasing EMI and crosstalk as well as altering signal waveforms. New routing design rules, such as making corners 30° instead of 45°, and more careful board fabrication techniques may become necessary as designs move above the 10 Gbps per lane threshold.

The move to higher frequencies will affect more than board fabrication and layout, however. Higher frequencies will also impose new requirements on signal timing, signal rise-time, electrical distance, and waveform shape if developers are to retain the mix-and-match system design approach that makes standards-based system design effective.

For interoperability to be achievable at data rates above 10 Gbps, organizations such as PICMG will need to carefully define a variety of signal and design parameters in their specifications. Some of the key parameters that will need consideration include:

- Interconnect signal attenuation
- Eye diagram
- Jitter
- Input clock recovery
- Chip input/output pre-emphasis (PE)
- Equalization (EQ)

Even slight variations in these parameters from device to device and lane to lane can shift the timing of signals a significant fraction of a clock cycle and affect the Bit Error Rate (BER) of a lane/channel. Finally, signal rise times will require tight control as signal rates increase in order to ensure control of system timing (see Figure 2).

In defining signal and design parameters, specifications will also need to account for the increased location dependency that comes with higher frequencies. Even subtle differences in attributes such as routing length and trace impedance become increasingly significant as signal speeds rise. To ensure mix-and-match interoperability, then, design specifications may need to account for the specific backplane slot that a board is to occupy as well as introduce a method to obtain and control the PE and EQ of the devices connected to the lanes.

Designers must also address fabrication standards. The material used to fabricate

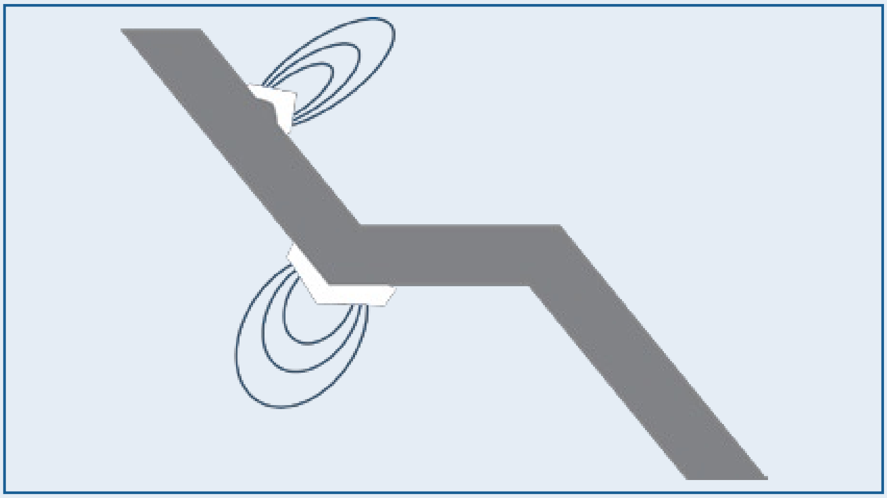

Figure 1

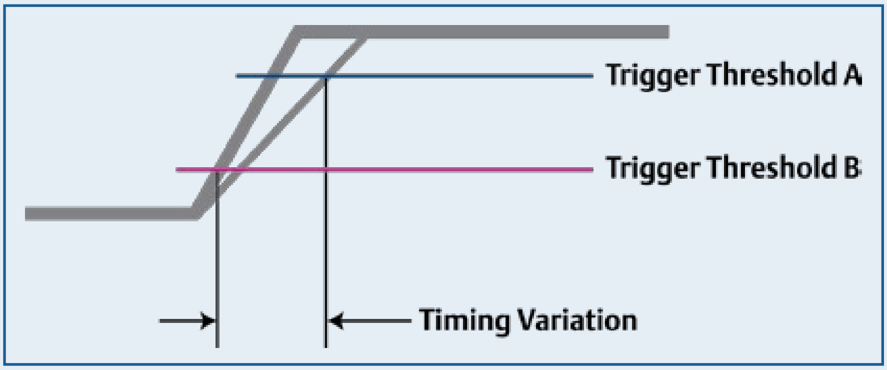

Figure 2

the board, the thickness and composition of metal cladding, and the spacing between layers can all affect the trace characteristics. Controlling these parameters under specification ensures that timing characteristics are sufficiently uniform from one board to another. However current specifications are too detailed and stringent. It is extremely difficult to attain compliance yet avoid adding cost to the design.

Specifications need work

Some of these parameters are already incorporated into current specifications. The AMC module specifications from PICMG, for instance, include design parameters that ensure its proper operation at signal speeds as fast as 12.5 Gbps per lane. Establishing specifications for other system components will help achieve interoperability of standards-based designs at higher frequencies.

Design tools may also need to be modified, and the industry will need to create new design rules for high frequency and incorporate these into the tools. Developing new routing techniques will help avoid the issues of electrical phenomena such as skin effect, dielectric loss, and impedance mismatches. These are much more prevalent at higher frequencies, and it becomes critical for engineers to model and simulate these phenomena more accurately.

Early efforts are already underway to address the challenges that higher frequency signals bring to standards-based design. The Interconnect Channel Characterization Subcommittee of PICMG, established in September 2006, is developing ground rules and definitions to be used in characterizing transmission, reflection, and crosstalk performance in backplane and mezzanine carrier interconnects. The committee aims to define the channel parameters to be measured or analyzed as well as the methods for doing so. Its charter calls for it to address:

- Definition of interfaces at which measurements are made or characteristics computed
- Test equipment, fixtures, and PCB test coupons
- Details of measurement procedure
- Data formats
- Techniques for de-embedding components of the channel
- Techniques for validating measurement based models, i.e., passivity and causality
- Definitions that allow reasonable compliance testing
- Boundary definitions for different paths
- Define information regarding limitations or proper usage, i.e., maximum data rate/rise times that are supported by the models

Such efforts are only a beginning, however. Other design details still need to be addressed, such as SERDES I/O Configuration. New functionality may need to be defined. The design of high data rate system channel interfaces according to standards/specifications does not currently cover the individual characteristics of the chip transmitter/receiver characteristics. Thus work will be needed to address how such standard designs handle such dependency.

Crossing an interoperability threshold

One way of handling location dependencies might be to give the system controller the ability to inform modules what the channel transmitter and receiver PE and EQ technology is and, importantly, how to control it. With this information, along with the signal attenuation suffered (at a given bit rate) for the channel, the system should be able to configure SERDES channels in different physical locations to run reliably and at the required BER. In MicroTCA systems, for instance, this functionality could be incorporated into the MicroTCA Carrier Hub (MCH) as part of its electronic keying function. Modules would have to be able to configure and control its backplane interfaces to allow for different positions in the backplane. An MCH (see Figure 3, courtesy Emerson), then, would be able to instruct a module as to which parameters to use for interoperability.

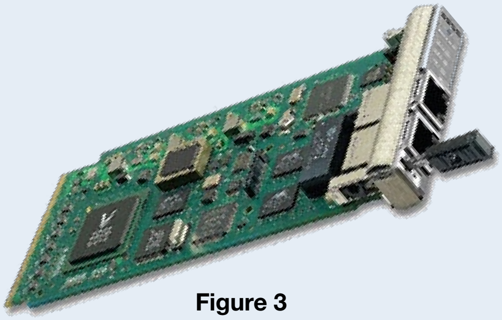

Figure 3

The specific approaches needed to handle location dependencies and other challenges that higher signal rates raise have yet to be developed. The need to address these challenges, however, is clear. Increasing demand for services is driving applications to utilize faster signal rates. This, in turn, is driving backplane signaling speeds ever higher. As speeds rise above 10 Gbps, signals will cross a threshold where current specifications will prove inadequate for ensuring interoperability among standards-based designs.

The industry should begin developing new or enhanced specifications and design tools to address the challenges of higher signal rates. Without such improvements, the guarantees of interoperability that allow system developers to readily create solutions by combining off-the-shelf products will be compromised. As backplane speeds approach 100 Gbps, nothing can be taken for granted.

***Stuart Jamieson**, Director of Industry Relations/Architect with Emerson Network Power, Embedded Computing, represents Emerson on PICMG committees and the SCOPE organization, and previously served as a CP-TA Board member (Treasurer). He brings over 18 years of experience in hardware, protocols, embedded software, and specification development to these groups. Within Emerson, he played a key role in the development of the technology central to Emerson's bundled networking solutions. Stuart's positions within Emerson have included Director of Business Development, Director of Advanced Technology, and Architect. He is the Draft Editor for the PICMG Interconnect Channel Characterization Subcommittee, is the author of the introduction section for the new PICMG Ruggedized MicroTCA specification, and served as the Draft Editor for the PICMG MicroTCA Specification. Stuart graduated from the Heriot-Watt University in 1989 with a 1st Class Honors degree in Electrical and Electronic Engineering and again in 1992 with an IBM-sponsored Master of Philosophy.*

Emerson Network Power Embedded Computing
Stuart.Jamieson@Emerson.com • www.emersonembeddedcomputing.com