

# CompactPCI Express: Protecting CompactPCI investments made over the last 10 years



By Andrew Brown

*Very recently, the CompactPCI Express specification was finalized and made public for both 3U and 6U board formats. This standard actually permits the use of current 32-bit, parallel CompactPCI peripheral devices in hybrid slots. Hence, "old" can mix with new, bridging the generation gap, without scrapping investments in CompactPCI technology made over the past 10 years and without losing out on the obvious advantages presented by this modern serial bus architecture.*

In the early 1990s, Intel developed the PCI Peripheral Component Interconnect (PCI) bus because the bus architectures of the day, Industry Standard Architecture (ISA) or Extended Industry Standard Architecture (EISA), with their industrial counterparts, SMP or ISA96, were fast coming to the end of their performance spectrum. All the more aggravating was the need to license the EISA bus. The desire for greatly improved data transfer rates and multiprocessor support spurred development of the PCI bus. In addition, when compared with the EISA bus, the costs had to be kept to a minimum without compromising user friendliness through software configuration. Since the application areas for the PCI bus were to be as wide-ranging as the technology of the time would allow, the concept had to cater to a processor-independent environment that was also license-free. What emerged was a specification with a multivendor capability that had a well-defined electrical and mechanical interface and rigid bus protocol. Upon completion of the specification, the PCI bus was handed over to the PCI-SIG, who ensured that further developments would remain multivendor friendly and license-free. Major advances to the original specification included the doubling of the data bandwidth (from 32-bit to 64-bit) and that of the bus frequency (from 33 MHz to 64 MHz). Then, in 1995, just a few years after its introduction, the standard was adopted for

industry in the form of CompactPCI. Today, these properties permit maximum data throughput from 133 megabytes per second (MBps) to 533 MBps.

PCI Express, developed again by Intel, was originally termed 3rd Generation I/O (3GIO) and is a completely new bus system where data is transferred via high-speed, point-to-point serial links known as lanes. (Figure 1) In the PCI Express world, each lane comprises a pair of differential conductors with one pair for data transmit and the other for data receive. In addition, these lanes can be bundled to a maximum 32 lanes per channel. Each lane then is able to transfer data at a 250 MBps rate in each direction; with all 32 lanes bundled together, this data transfer becomes an impressive 8 gigabytes per second (GBps) (or 16 GBps in both directions) total. CompactPCI Express, by comparison, supports bus structures with 4 to 16 lanes per channel enabling data transfers up to 4 GBps. This represents a massive improvement on the current 133 MBps offered by today's CompactPCI. Compared to other parallel bus structures, CompactPCI Express is fully bidirectional, permitting simultaneous data transmission

and reception, effectively doubling the 250 MBps data throughput to 500 MBps. The syntax describing this architecture is as follows: (channels) x (lanes) – so 2x4 lanes describes two independent CompactPCI Express channels with four bundled lanes per channel. If a CompactPCI Express peripheral board cannot administer all available lanes of the system board, then the unused lanes will be automatically deactivated during initialization.

Note that the method of data transfer in a CompactPCI Express environment makes it ideal for PCB manufacture using FR4 materials, and even permits conductor lengths up to 50 cm. Being serial in nature, CompactPCI Express:

- Possesses CRC checksum algorithms for error recognition and correction
- Is AC coupled (no ground loops)
- Has native hot plug support

CompactPCI Express extension boards can be replaced without the need to remove the main power first. Because CompactPCI Express supports point-to-point connectivity only, interfacing con-

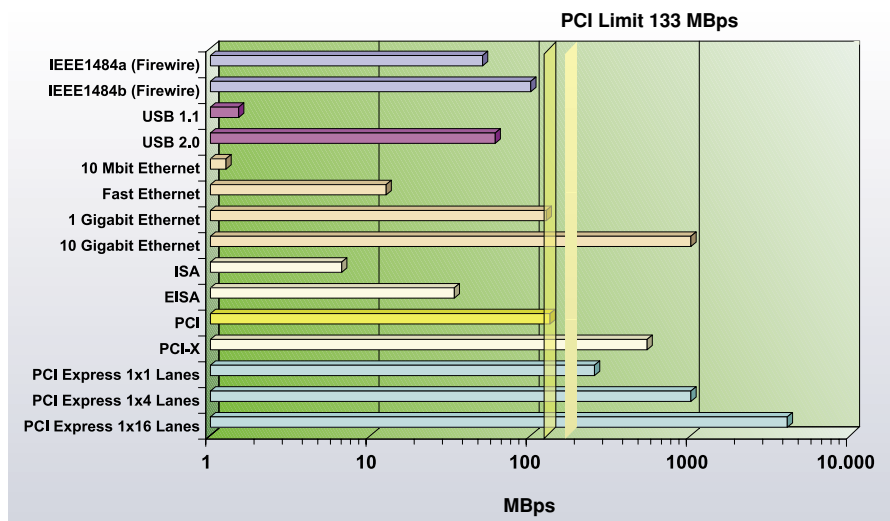


Figure 1

ventional 32-bit parallel CompactPCI boards requires *switches*. The transition between PCI and PCI Express is transparent as far as the operating system is concerned, and assuming the PCI board conforms to the PCI 2.2 specification. To use the advanced features inherent in the PCI Express standard, such as extended error handling or power management, the OS must be able to address them directly. Otherwise the existing PCI interrupts are recognized, and the device drivers remain unaltered. The first 256 bytes of configuration space are identical to the current PCI registers, and because the operating system views the PCI Express *root* or switch as a virtual PCI bridge, even older operating systems can configure CompactPCI Express devices. The BIOS must however support PCI Express completely, since such devices have a relatively large configuration space.

### Capitalizing on PCI Express in an industrial environment

To take advantage of PCI Express in an industrial environment necessitated the introduction of specially tailored connectors. In total, three additional connectors have been developed to sit alongside the well-known CompactPCI connectors. Data transmission on the high-frequency channels takes place through differential Advanced Differential Fabric (ADF) connectors. These have an intrinsic impedance of 100 Ohm and an input attenuation of < 1 dB at 3 GHz. Since these connectors are used primarily for the HF signals, additional power connectors are required. These come in the form of the Universal Power Connector (UPM), which has seven individual contacts for the system board:

- One 3.3 V
- One 5.0 V
- Two 12.0 V
- Three GND

Each contact can be loaded at 15 A, which in theory at least, permits the system board to draw a maximum of 340 W. By contrast to CompactPCI, where, in general, the main board power is derived from the 5 V line, in a CompactPCI Express world the main power is drawn from the 12 V line. The core voltages on a CPU board are thus generated from it and, as a consequence, have a better signal. The -12 V signal is no longer supported on the pure CompactPCI Express slots, but is supported in hybrid configurations for legacy

CompactPCI devices – assuming the PSU is capable of generating this signal.

A specially defined Enriched Hard Metric (eHM) connector is used for carrying additional I/O signals and some power. This connector is keyed, thereby preventing for example, PXI boards from being used in a configuration where rear I/O is required. In total, four different key combinations are possible defining unused I/O pins, rear I/O, extended rear I/O, PLX extensions, and bus orientated sideband signals. All combinations support Hot Swap and Wake Up functions. Except for the extended rear I/O option, additional 12 V, 3.3 V (2 A), and 5 V<sub>aux</sub> (1A) power lines are available. Here, the CompactPCI Express specification deviates slightly to that of the PCI Express specification in which V<sub>aux</sub> is 3.3 V and the maximum loading just 375 mA. In the CompactPCI Express specification, the 5 V signal for main board power is no longer available. In a CompactPCI Express environment, the V<sub>aux</sub> is primarily used for Wake Up tasks, and is present even if the system has switched off the main power.

Two approaches apply to switching on or switching off a CompactPCI Express system. This can take place through a control signal from the PSU, or via a Wake Up event from a timer interrupt or some other external source. Here, the power consumption of the system can be regulated or reduced while in operation, allowing a CompactPCI Express system to be fully active only on those occasions where it is actually required. The second method is through the usual mechanical on/off switch. The electrical, mechanical, and climatic properties of all connectors conform to IEC-60512.

### 3U advantages

As with existing CompactPCI systems, all major bus signals are present in the 3U form factor, giving two major advantages over VME systems for example. One, high-performance systems can be created in a highly compact 3U format with the only restriction being the physical PCB surface area compared with the 6U systems. Given today's integration density, and serial CompactPCI Express bus system, this presents zero drawbacks. Very few contacts are required when interfacing, for example, a 64-bit parallel device. The second advantage is that those standardized extensions pertaining to telecom, for

example, present in the upper region of 6U boards, do not have to be affected by the introduction of CompactPCI Express. Hence, existing standards are respected, and current installations profit from this approach.

The major changes that have taken place in CompactPCI Express compared with CompactPCI are concerned with the 3U form factor. Connectors and their use in the 6U portion remain the same and conform therefore to PICMG 2.0. It's the bus in the 3U region that has undergone the most change. Also, CompactPCI Express vastly improves upon the power consumption permitted by individual slots when compared with the requirements the PCI Express specification details. Here, for example, the power is limited by the consumption of the board occupying each slot. In the PCI Express model, power consumption is very much regulated and linked with the number of bundled lanes. So, a PCI Express board configured with 1x1 lanes can, according to the specification, consume just 10 W at startup. By comparison, in the CompactPCI Express model, the lowest power consumption at startup is in the 30 W range.

The CompactPCI Express specification defines six different types of slots that can be used in backplane manufacture. Remaining from the current CompactPCI specification are the power connector for the PSU and the *legacy slot* for existing parallel-based peripheral boards conforming to the CompactPCI PICMG 2.0 specification. The CompactPCI Express specification introduces a number of new connectors to the system slot. Power is obtained through the seven-pin UPM connector. In addition, ADF and eHM connectors are used for the CompactPCI Express channels where they also serve the rear I/O and provide additional power outlets. The eHM connector on the system slot, need not, according to the CompactPCI Express specification, have pins allocated for power. All pins of this connector can be reserved for extended rear I/O tasks. The system slot (Master) presents the CompactPCI Express signals either as four channels, that is, 4x4 lanes or two channels with 1x8 and 1x16 lanes. As an option, a combination of 1x8 and 1x16 is also possible. However, the system slot must, under all circumstances, support as a minimum, the 4x4 lane scheme. System slots support-

ing 1x8 or 1x16 lanes are, in this case, only provided with 2x4 lanes. A *slotpin*, present in the system slot, defines which of the two combinations is present. The CompactPCI Express specification defines only the minimum number of PCI Express channels. Instead of, for example, the presence of the complete 4x4 lanes, at least one 4x1 lane must be present, (or in other words, one channel with at least one lane). Because the system slot does not support parallel bus architectures, a bridge is required when mapping the parallel CompactPCI bus to a single CompactPCI Express channel.

The specification allows for four different kinds of peripheral board. The first is identical to that of the current CompactPCI architecture. Then there are two pure CompactPCI Express slots and one hybrid slot in which both conventional CompactPCI connectors and Type 2 CompactPCI Express connectors are present, as Figure 2 shows. In this slot, standard 32-bit CompactPCI peripheral boards can be used or the newer CompactPCI Express boards (Figures 3A and 3B). All boards have the possibility of tapping into the eHM connector present in this slot, so that even legacy CompactPCI boards can take advantage of Hot Swap or even Wake Up functions.

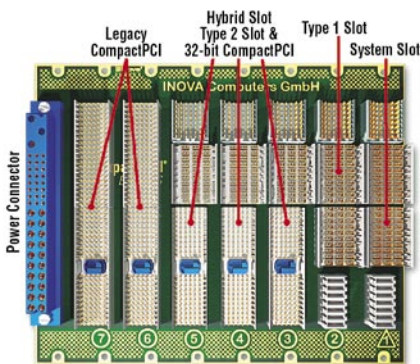


Figure 2



Figure 3a

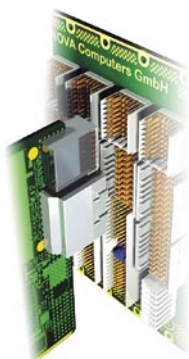


Figure 3b

The Type 1 peripheral slot has the same connector layout as the system slot with 2 PCI Express channels configured for either 1x4 or 1x16 communication. CPUs can be placed in this peripheral slot as long as they have a nontransparent bridge or are capable of Advanced Switching. Here, two PCI Express channels are present and observe the 1x4 lane and 1x16 lane scheme whereby the 1x4 lane scheme is mandatory while the second channel with 1x16 lane is optional.

Type 2 peripheral slots have ADF and eHM connectors with board power being supplied through the eHM connector only. This slot has just one PCI Express channel present with 1x4 lanes. Type 2 boards can work in a Type 1 environment but not conversely, since the UPM connector for the main power is missing in Type 2 slots. Type 1 slots are generally reserved for power-hungry boards, so the power rating of the eHM connector may not be sufficient.

By contrast to parallel bus systems where only two devices can communicate on the same bus, CompactPCI Express permits all devices to communicate simultaneously. Hence the complete bandwidth is available at all times (Figure 4).

**Bridging the generation gap**

The *hybrid* slot is a combination between a Type 2 peripheral slot and a traditional

32-bit CompactPCI slot. This is a universal type of slot. Either CompactPCI or CompactPCI Express can be positioned here. Even PXI architectures are supported and have their dedicated signals routed through the eHM connector. Hence, new system designs can take advantage of existing CompactPCI technology without losing out on the advantages presented by the newer CompactPCI Express technology. Combining both new and old in this way is an ideal method of bridging the generation gap. The advantages of CompactPCI Express, such as cost reduction through a simple serial bus structure, high data transfer rates, and future-proof design, are combined with backward compatibility with existing CompactPCI technology. Figure 5 shows that the PCI compatible layer structure of CompactPCI Express allows it to be used with any compatible operation system.

Since the system CPU can directly control just four CompactPCI Express slots, *switchboards* are used to distribute control if more slots are required. Hence, backplanes can have slots dedicated to one or more switchboards. In a 3U CompactPCI Express environment, up to a further seven slots can be addressed using the 1x4 lanes configuration while in a 6U environment, switchboards can have 18x4 lanes or even 8x8 lanes.

The backplane configuration, that is, the

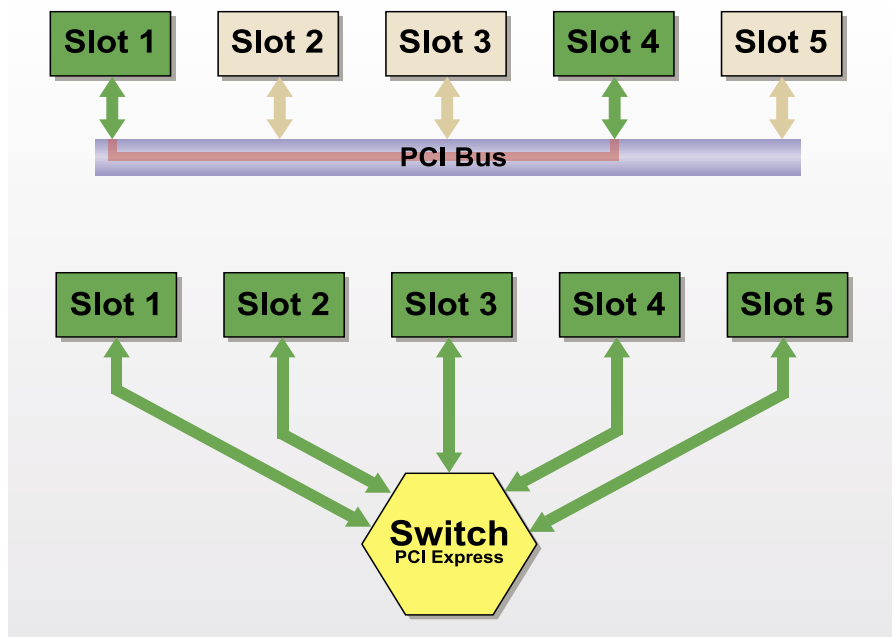


Figure 4

number and nature of the available slots together with the channel and lane architecture, are stored in an EEPROM device. Besides this general description of the backplane, the EEPROM stores additional information on, for example, the manufacturer, date of manufacture, lot number, and serial number.

CompactPCI Express is a universal, high-performance and future-oriented bus system for the industrial marketplace. Apart from offering just high-speed serial data transfers, CompactPCI Express, with its asynchronous communication, is equipped with CRC checksum algorithms for error recognition and correction, and provides native hot plug functions – prerequisites for a universal bus. It is expected that the first operating system to truly take advantage of all these features will be Microsoft's *Longhorn*, the successor to Windows XP, in which native support for PCI Express is embedded and hot plug of peripherals are permitted without extra, and often expensive, software overhead.

Because of the widespread distribution of this technology in the desktop marketplace, the price of the individual PCI Express components is expected to be even lower than that of the currently available PCI devices. CompactPCI Express combines the very latest communication technology with the platform compatibility and stability of CompactPCI, giving developers

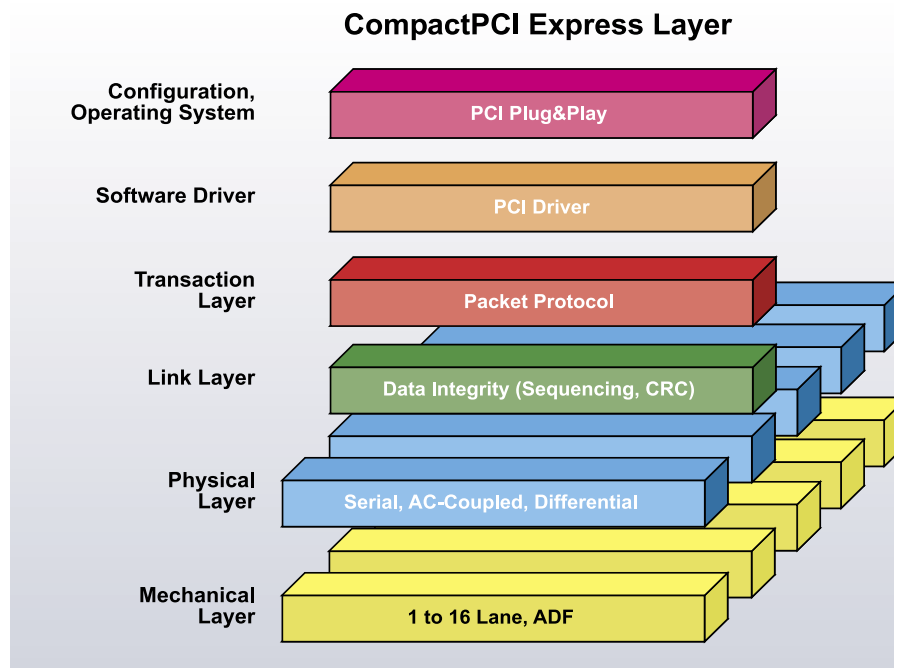


Figure 5

reason enough to use it as the basis in all conceivable industrial applications.

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