

Next-generation networks

Custom high-speed CompactPCI backplane

What do you do when you prefer the idea of COTS-based development, but you already have an existing design? You now have to squeeze even more performance out of the system... how can you get the best of both worlds, COTS and custom configuration from a single backplane?

The benefits of COTS-based equipment has been a much discussed subject for a number of years. After decades of custom designed equipment for military systems based around the perceived special needs, the alternative viewpoint of standards, availability, and the potentially easier route for upgrading systems has made significant inroads into rugged system designs.

The established base for this lies with VME, having been the pre-eminent standard when the move to COTS equipment started. With the ability for users to define the pin-out functionality of the outer rows of the J2 connector, the opportunity exists for specialist user applications while the basic bus structure remains unchanged.

Over the years, Mektron Systems Ltd has designed a number of these special boards, including full-military specification (MIL-P-55110) backplanes for use in both conduction and convection cooled systems.

CompactPCI has boosted this level of user definition with its greater potential for custom I/O, the basic architecture only requiring a smaller fraction of the space available on the edge of a standard 6U card format.

Increasing bandwidth can be achieved by greater parallelism (wider data paths) or faster edge rates or a combination of both. There are a number of considerations when attempting to transport data faster. The use of wide paths brings a number of issues, with greater switching currents and greater physical distances across a connector field causing skew in the signal timing.

Higher speed switching relies on improved signal fidelity. One of the reasons CompactPCI basic pin-out definition provided regular ground patterning along the edge of the connector field was to give a higher ground/signal ratio. For even greater improvement it is possible to form a quasi co-axial connector by assigning ground pins throughout the pin field. This gives good shielding between signal lines and provides a controlled ground return path, but at the sacrifice of pins.

Conventional systems, whether based or point-to-point rely on the return current via the ground path. Thus, for any signal to be transmitted, an equivalent return signal is required. If the return path is tortuous, this will degrade the signal and ultimately limit the data rate. This may be as a result of inductance in the ground plane layout of the backplane causing ground "bounce," or the potential for noise to be induced to the data line when the return path is physically separated from the signal path, creating a loop area.

Differential mode transmission minimizes these problems and to achieve the customers' requirements, the latest version of the system has embodied a number of changes to achieve even higher speed operation. The chosen solution was to implement a dedicated high-speed path between two adjacent boards within a defined link area.

Backplane construction

The backplane considered here is used in a rugged application. Initially developed by Mektron Systems Ltd, the system was based around a custom CompactPCI four-slot standard backplane (see Figure 1). Despite the relatively high bandwidth inherent in the system, subsequent development of the target architecture called for a number of new high-speed data paths. The signal types used on this backplane fell into the following categories:

- CompactPCI signaling
- Low Voltage Differential Signaling (LVDS)

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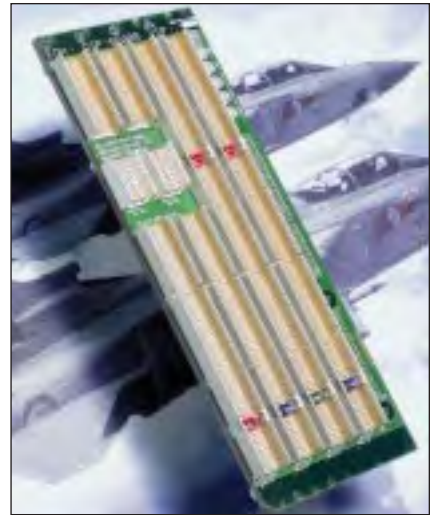


Figure 1

- Analog
- High-speed serial bus

All of these signal types need to be handled on the one board, with a range of characteristic impedances and the need for some special signal handling. One of the goals was to retain conventional FR4 material for the board construction. Alternative materials, with lower dielectric values, typically carry a cost penalty and a restriction on the number of PCB fabrication houses that can handle the processing.

Performance dictated that all signal layers be buried, using a strip line construction to guarantee controlled impedance and separation from extraneous noise. The final construction was achieved in a board with a modest 14 layers.

Connectors

The P4 connector used in this application is purpose built for very high-speed differential transmission. The ERmet ZD range of connectors is based around the 2mm hard metric standard (IEC 061076-4-101). The heart of the system is a pair of pins with an adjacent "L" shaped screen around each pair (see Figure 2). Internally, the female half has the tracking arranged to minimize the track differential length

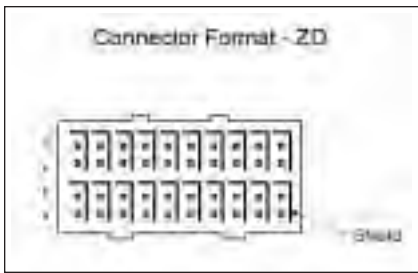


Figure 2

(on the male mating half, trace equalization is performed in the backplane layout). The end result is a connector capable of transmitting data at 5 Gigabits/sec, ideally suited to the types of signals we needed to transport. Figure 3 shows an ERmet connector in P4 position.



Figure 3

Signal types

CompactPCI: Conventional signaling using single ended drivers and receivers. The CompactPCI bus is based around a 65 ohm line. Unlike previous bus architectures, CompactPCI utilizes a series termination resistor on the daughter board, thus doing away with the pull-up/pull-down termination seen at the end of the longer TTL backplanes (VME/Multibus II etc.). The majority of interconnects on the board were identical to the existing standard product.

LVDS: As the name implies, the data and its complement are transmitted simultaneously over a closely matched pair of lines (see Figure 4). Design rules for LVDS call for a number of special considerations:

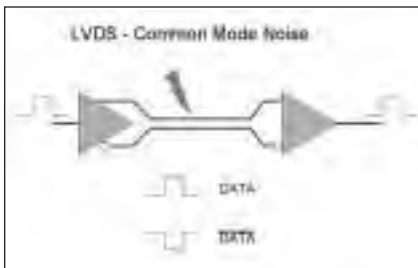


Figure 4

- Isolation of LVDS signals from TTL/CMOS signals, normally achieved by having a dedicated tracking layer.

- A differential impedance (Z_{oe}), typically 100 ohms, is required between the pair of traces. This requires a geometry similar to the 60 ohms used in single ended transmission (Z_{oe})

$$Z_{oo} = 2 \times Z_{oe} (1 - 0.374 e^{-2.9 s/h})$$

Where "s" is the separation between the traces and "h" is the dielectric separation (see Figure 5).

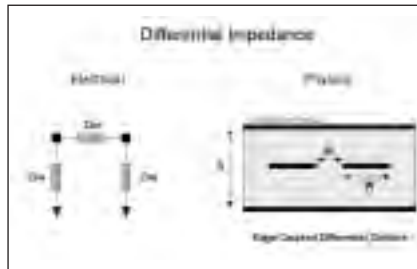


Figure 5

- Pairs of lines can be edge coupled (side by side) or broadside (stacked vertically above each other) between the reference layers. In this application, edge-coupled format was chosen.
- The paired lines are kept close together for a number of reasons. This keeps the line length as close as possible (minimizing signal skew) and keeps the loop area as small as possible. Good practice says that the next nearest pair should be the greater of twice the separation or twice the trace width away.
- High-speed signal routing for any logic family avoids sharp trace direction changes. Any rapid change causes a discontinuity, which results in a proportion of the signal being reflected back towards the source. Curved traces are ideal, but more typically 45° changes are used. If using right-angled changes, an angled chamfer offers improvement (see Figure 6).

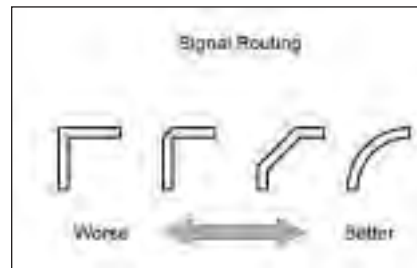


Figure 6

- For ultimate performance, traces entering the connector field should be routed on the opposite side to the connector. This way the via in the board

is part of the trace. If tracked on the connector side, the via appears as a short stub at very high frequencies, resulting in unwanted reflections (see Figure 7).

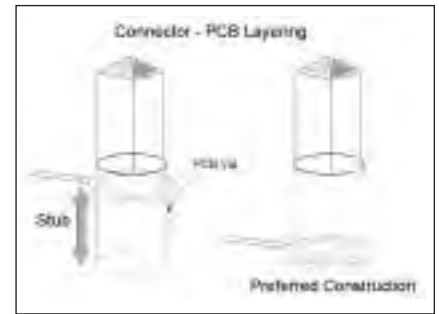


Figure 7

Analog: The special handling of the analog portion of the data required modification of the geometry of the (single ended) lines to achieve a 75 ohm characteristic impedance. Reduction of trace width or increasing dielectric separation (or a combination of both) will increase the intrinsic impedance of a line. Of greater significance in the design of this board was the need to maintain an analog ground reference, quite independent of the logic ground.

High-speed serial bus: A number of techniques described above were used to create this dedicated bus. Based around a 100 ohm differential system, the lines were additionally protected with shielding tracks. These need to be either side of the differential pair to achieve a balanced shield and to be effective must have a frequent connection to the ground plane. Their position needs to be at least at a distance of twice the separation of the pair that they are designed to protect. Also needing special attention is the effect of bringing a ground protection trace adjacent to a signal pair. This requires special factoring in to the design equation if the measured impedance is not to fall below the target figure.

Power planes

The construction of the board used common copper weights, with power planes fabricated from 2oz copper and the signals carried on 1oz planes. To achieve the construction in a minimum layer count the design utilized split planes, the signals traces are related to their adjacent reference planes. By splitting the plane, a single layer can act as different references for different signal types.

Conclusion

The end result was a backplane that met the various goals, bringing together a COTS based CompactPCI implementation, based on a previous design that would accommodate standard boards, while extending the capability of the system with a special high-speed area. Sometimes it is possible to have the best of both worlds.



Martin Blake has been actively involved in high performance bus-based backplanes and associated enclosure technology for in excess of sixteen years. During this time he has occupied a number of senior engineering, sales, and managerial positions in British and American companies including British Aerospace, Teradyne, Vero Electronics, and APW Electronics.

Martin is a member of the IEE and IEEE and has been a member of various standards committees for bus architectures (specializing in backplane design) and packaging standards since 1986. He was a member of the VITA Technical Committee chairing the Backplane Sub-Committee prior to it becoming the VITA Standards Organization (VSO).

Martin graduated from University of Bath in Electrical and Electronic Engineering and is a Chartered Engineer. He is currently Business Development Manager with Mektron Systems Limited / Miltron Systems Inc.

I N F O

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