

# High performance view: CompactPCI Express

By *Steve Cooper*

*The next generation of CompactPCI is beginning to roll out in the form of CompactPCI Express. This upgraded standard includes substantial performance increases, compatibility with both legacy products and the latest office PC technologies, and a unification of backplane buses into a single bus that supports both CPU-to-I/O and CPU-to-CPU communications. The first products based on this new standard, including those in the CompactPCI Express Product Guide that follows, are now beginning to appear, and represent the first look into this powerful architecture of the future.*

## Historical perspective

The PICMG standards body developed CompactPCI in 1996 as a standard bus structure that combines the cost-effective PC bus architecture (PCI) with the popular Eurocard industrial board form factor. This combination quickly became the world's most popular bus structure for industrial, communications, military, and test systems where PCI is used in a rugged form factor. In 2005, PICMG defined a new CompactPCI specification that replaces the PCI bus with the new PCI Express bus.

The addition of PCI Express to the CompactPCI standard allows CompactPCI Express to utilize the latest PC market components, extending the bus architecture's useful lifespan for at least the next decade.

Products based on the new standard are now becoming available, with many more product announcements anticipated over the next several months and years.

## Benefits of CompactPCI Express

CompactPCI Express brings several higher-performance benefits to traditional CompactPCI applications, including:

- Bus transfer speeds increase 10-50 times
- PCI Express connections are all point-to-point, eliminating arbitration delays
- CPU-to-CPU transfers can occur at the full bus bandwidth
- No need to run relatively slow Ethernet through the backplane

## Compatibility with legacy boards and chassis

Hybrid systems that include a mix of CompactPCI Express as well as legacy CompactPCI slots are easily implemented. CompactPCI and CompactPCI Express boards are the same form factor and include the same faceplates and other mounting hardware, so existing chassis need only upgrade their backplane to be used in CompactPCI Express.

## Low costs through access to the latest commodity components

The latest I/O components that include native PCI Express interfaces can be easily designed into new CompactPCI Express

I/O boards. Figure 1 shows a dual Gigabit Ethernet component with a native PCI Express interface in the new CompactPCI Express form factor.

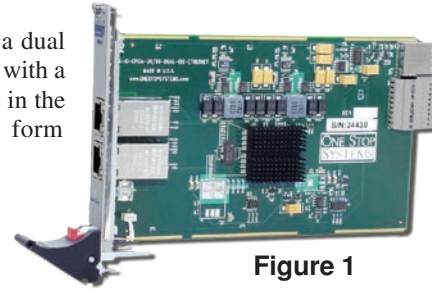


Figure 1

## New capability to run PCI Express over cable

The CompactPCI Express architecture enables attached PCs to control a CompactPCI Express subsystem at full speed and with full software transparency.

## Bus unification, improved multiprocessing, and fault tolerance

Incorporating Advanced Switching (ASI) extensions to PCI Express, CompactPCI Express supports both CPU-to-I/O and CPU-to-CPU communications over the common backplane, creating a cost-effective upgrade path for PICMG 2.16 applications.

## CompactPCI Express basics

CompactPCI Express replaces the P1 and P2 connectors used in CompactPCI with four connectors that provide the new PCI Express bus as well as enhanced power capabilities to each board, as shown in Figure 2. The bottom connector provides high current connections for incoming power; the second and third connectors provide the PCI Express differential pairs for multiple PCI Express buses to be routed from each board to the backplane. The top connector provides utility pins for user-defined rear I/O, PXI extensions for instrumentation, and power input for the low-cost Type II I/O modules.

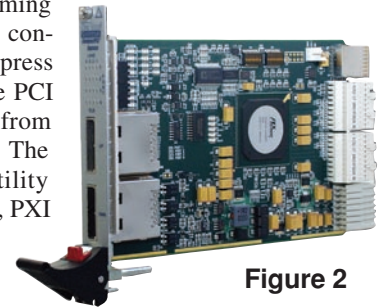


Figure 2

System slot boards within CompactPCI Express drive either two or four PCI Express buses onto the backplane.

This allows the direct connection of up to four I/O slots. For larger configurations, a switch is needed to expand the PCI Express fan out to additional I/O slots. Figure 3 shows an eight-port switch board.

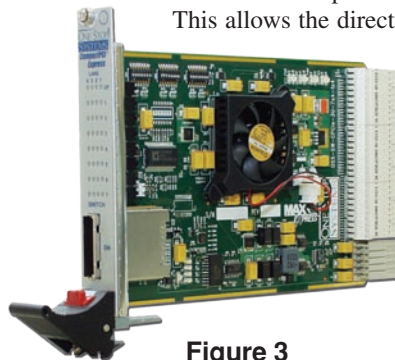


Figure 3

A bridge board can connect one PCI Express port to traditional PCI, enabling hybrid systems that contain a mix of CompactPCI Express and legacy CompactPCI slots. Figure 4 depicts a 6U CompactPCI Express backplane that supports this hybrid architecture.

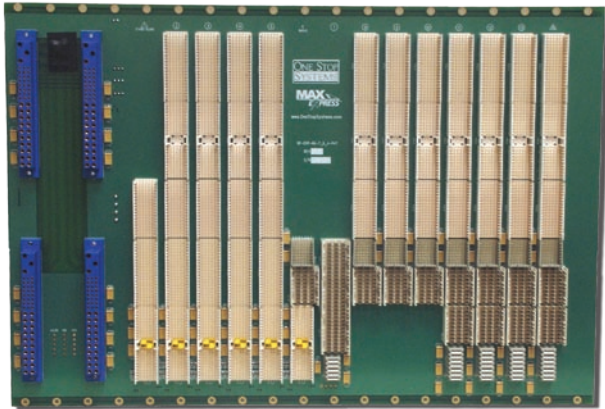


Figure 4

**Support for both internal and external CPU**

New PCI Express capabilities include running the bus at full performance with total software transparency over a cable as well as a backplane. For CompactPCI and CompactPCI Express systems, this transparency enables system configurations where the CPU element is external from the CompactPCI Express system. For example, it's possible to create a development system for CompactPCI Express that is based on an external PC attached via PCI Express over cable (Figure 5).



Figure 5

Deciding whether to have an attached PC versus an internal CPU involves several trade-offs. Attached PCs are often more robust, offering the latest CPU speeds, memory, and peripherals. Embedded PCs have the advantage of eliminating the second chassis, and providing a more consistent level of ruggedness. Often, designers will choose the convenience of an attached PC for development, and then transition to an embedded CPU board for production.

**Tree and network topologies**

CompactPCI Express supports both tree and network topologies. A tree architecture includes one CPU element connected to a number of I/O elements. This is the most cost-effective

topology and is suitable for many applications where a single CPU is needed.

CompactPCI Express also supports multi-CPU applications. These applications take advantage of the ASI PCI Express.

**ASI within CompactPCI Express**

ASI is an extension to PCI Express that allows CPU-to-CPU communication and dynamic I/O mapping to work on top of the basic PCI Express functionality. For multi-CPU systems, this unifies the CPU-to-CPU communications bus and the I/O bus structure. This unification significantly improves performance, system cost, and fault tolerance.

Systems based on ASI within CompactPCI Express utilize the same CPU and I/O boards as tree architecture systems. A different switch board is needed, however, to provide the PCI Express-to-ASI bridges for the CPU boards and the ASI-based switch functionality.

**PICMG 2.16 solution for multiprocessing**

Both CompactPCI and CompactPCI Express have built-in flexibility via their P3, P4, and P5 connectors that are available for user-defined rear I/O and/or secondary buses or interconnects. Several uses for these connectors have become standardized. One of the most popular is PICMG 2.16, which defines how 1 GbE can be routed through the P3 connectors to a special 2.16 switch slot. This mechanism allows multiple CPU boards to intercommunicate via the Ethernet in a network topology. *Split backplane* solutions have extended this concept to allow multiple CPU domains (isolated CPU and I/O slots) to be integrated within a single system, with the CPU boards connected by Ethernet routed via 2.16.

**ASI as an upgrade path for 2.16 systems**

ASI within CompactPCI Express provides a particularly attractive upgrade path to 2.16-based systems. The advantages of ASI include 10-50 times higher performance, lower costs, and dynamic I/O mapping.

ASI performance depends on the lane width of the underlying PCI Express buses. Typical systems will include two independent x4 PCI Express bus interfaces from each CPU board. Each of these interfaces operates at 10 Gbps. Higher performance is achievable by boards that utilize x8 or x16 interfaces. The move to Gen 2 timing, which is expected to become available in late 2007, will also increase performance.

Combining two buses (PCI and Ethernet in 2.16) into one PCI Express bus that performs both functions lowers costs. CPU boards don't need to drive the extra Ethernet ports into the backplane, and an expensive 2.16 switch board is eliminated. The CompactPCI Express with ASI solution does require its own switch board, but this function provides both the I/O board fan-out and multiprocessor switching functions.

Dynamic I/O mapping allows any PCI Express I/O function to be mapped to any CPU board, with the mapping changeable on the fly. This capability provides greater hardware configuration flexibility and enhanced fault tolerance. If a CPU board fails, a

different CPU board can be remapped to take over control of the I/O boards. This type of capability doesn't exist within 2.16 systems. In those systems, if the controlling CPU board goes down, all the I/O associated with that CPU also goes down.

### Conclusion

CompactPCI Express provides the advanced features of PCI Express in the CompactPCI form factor. In doing so, it extends the useable lifespan of the architecture for at least another decade. 🌐



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*Multibus and Multibus II architectures. Steve then joined RadiSys, a company specializing in embedded PC-compatible computers. He also served as vice president of sales and marketing, and later president and CEO, at I-Bus. Prior to founding One Stop Systems, Steve was president and COO for SBS Technologies. He holds a BSEE degree from the University of California, Santa Barbara.*

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