Selective memory: Keep these 10 considerations in mind for AdvancedTCA blade design

By Arthur Sainio

2006 is shaping up to be the year for AdvancedTCA blades. The telecom industry is adopting open standards-based building blocks in place of proprietary systems, and AdvancedTCA blades will likely be the form factor of choice for next-generation carrier grade communications equipment. While AdvancedTCA blades have a standard architecture, they do not have standard memory requirements. Designers choosing AdvancedTCA blade memory need to consider many options and weigh the design/cost trade-offs carefully. Here are 10 key considerations to keep in mind when planning an AdvancedTCA blade design.

1 Technology type

For AdvancedTCA blades, the two main memory choices are DDR1 or DDR2 (Figure 1 shows DDR2 modules). The market transition to DDR2 is happening now; however, DDR1 still has a long life ahead. Typically the memory technology decision depends on the processor and chipset, but it is helpful to consider product life cycles and where they align with memory trends.

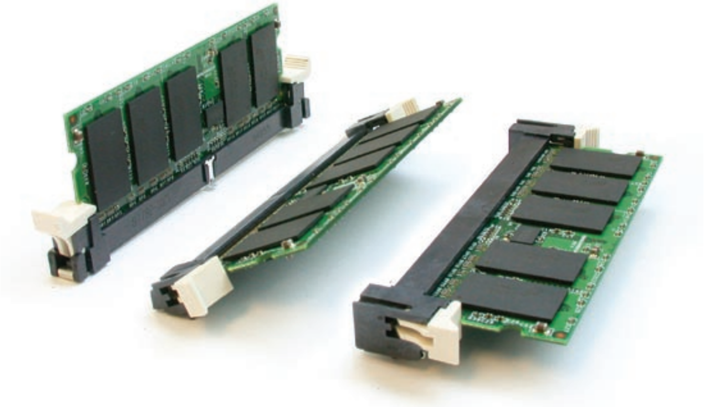

Figure 1

2 Form factor

The increase in AdvancedTCA-standard blades has led to a wider variety of available small module solutions. Table 1 shows the best module types for AdvancedTCA blades.

3 Configuration

The processor and chipset interfaces typically define module configurations, but designers can usually select from registered, unbuffered, unbuffered with ECC, and unbuffered with ECC/PLL clock driver. With unbuffered memory, the chipset interfaces directly with the memory, whereas with registered memory, registers hold data for a defined number of clock cycles.

After determining the module type, it is time to select a configuration. Common module data widths include:

- x72
- x64
- x32
- x16

Multiple DRAM combinations support these configurations.

4 Connectors

Currently, there are four basic connector options:

- Vertical
- Right angle
- Horizontal (notebook type)
- Angled

With AdvancedTCA blades, it is common to use 244-pin right angle mini-DIMM connectors that allow for low height as well as space underneath for extra passives. Vertical connectors in combination VLP modules can also be used to save board space and meet sub-1U height requirements. Finally, butterfly pairs of SODIMM connectors can be used to achieve high density and still accommodate a mezzanine card on top.

5 Power consumption

When evaluating the thermal efficiencies of memory subsystems, consider such factors as DRAM power consumption, system airflow, DIMM pitch, DIMM thickness, and whether a heat sink will be required. Power consumption will vary depending on the type of DRAM, but using modules designed with 8- or 16-bit wide DRAMs can typically lower consumption.

Technology	Module Type	Max. Density	# of Pins
DDR1	VLP Registered DIMM	4 GB	184
DDR1	SODIMM – Unbuffered, ECC	2 GB	200
DDR1	SODIMM – Unbuffered	2 GB	200
DDR2	VLP DIMM – Registered	4 GB	240
DDR2	Mini-DIMM – Registered	2 GB	244
DDR2	VLP Mini-DIMM - Registered	1 GB	244
DDR2	Mini-DIMM – Unbuffered	1 GB	244
DDR2	VLP Mini-DIMM - Unbuffered	1 GB	244
DDR2	Mini-DIMM – Unbuffered, ECC	1 GB	200
DDR2	SO-CDIMM – Unbuffered ECC	1 GB	200
DDR2	SO-RDIMM – Registered	1 GB	200
DDR2	SODIMM – Unbuffered	2 GB	200

Table 1

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6 Density

Packet-processing AdvancedTCA blades typically require lower density ECC modules while network appliance type of AdvancedTCA blades require 2 GB to 4 GB registered modules. BGA package size variations directly affect module form factor cost and the need for stacking options.

7 Price

Memory modules are a cost-effective design option because they can be changed to accommodate prevailing DRAM densities and prices. The key is to make sure the system is designed to function with the widest set of options, including support for 1 Gb devices, faster speed grades, and single or multiple ranks. The idea is to set the basic systems priorities first (for example, performance, low power) then work to achieve the best cost efficiencies.

8 Standard or derivative modules

Derivative modules follow the JEDEC pinout and socket standards but have been customized to meet specific customer requirements. These requirements include reducing clock loading, adding an extra chip select so the density can be upgraded by stacking, and moving far-end termination onto the module to save board space. Derivative modules shorten design cycles and development costs as compared to fully custom memory modules, yet they allow system designers to gain competitive feature advantages.

9 Testing

Increased processor speeds, more processors, and larger memory capacity combined with decreased board space and reduced airflow have resulted in systems that run hotter and are more prone to single and multibit memory errors. Choosing modules with ECC and designing systems that support Chipkill can minimize the impact of memory errors on system functionality.

10 Trade-offs

Choosing memory demands careful consideration among all trade-offs: Cost, thermals, capacity, connector type, spacing, module form factor, and configuration – all need to be weighed based on the application and market requirements However, with careful planning, AdvancedTCA designers can get the most out of their memory choices.

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