MicroTCA backplanes pack extensive functionality into a small space

By Christian Ganninger

Christian details several features affecting MicroTCA backplane design choices.

All data transferred between individual AdvancedMC modules goes through the backplane. The backplane is also responsible for power distribution to the modules. And last but not least it contributes to the mechanical stability of the MicroTCA system. Its high data transfer rates and serial interconnections can cause the backplane design to be a challenge for the developer.

No parallel bus

Serial data transfer uses differential signal lines for packet-oriented data transfer. The backplane slots are not connected with a parallel bus, but with point-to-point connections. Thus, extremely high data transfer rates can be achieved. Current transfer rates range from 1 to 3 Gbps per differential signal pair, with 5, 6, and 8 Gbps being achieved in the near future. The MicroTCA standard stipulates transfer rates of up to 12.5 Gbps in order to make MicroTCA future proof. Schroff offers MicroTCA backplanes, such as that shown in Figure 1, which support popular protocols including 1 Gigabit and 10 Gigabit Ethernet, PCI Express, Serial RapidIO, and Serial ATA.

Different topologies

Backplanes designed to the PICMG MicroTCA specification can have up to 12 slots for AdvancedMC modules, one or two slots for MicroTCA Carrier Hubs (MCHs), and up to four slots for power modules. Like most AdvancedTCA backplanes, MicroTCA backplanes use a star-shaped network topology (as a rule star or dual star for redundancy) with one or two hub (MCH) slots. A full mesh topology, like foreseen for AdvancedTCA, is not planned for MicroTCA. The star-shaped topology causes very high routing density areas in the backplane near the MCHs. The MCHs in a MicroTCA system are connected to the backplane with up to four of the same connectors used for the AdvancedMCs mounted side-by-side. Almost all of the pins on the MCH connectors are occupied. With a narrow connector of approximately 75 mm, these 680 signals have to be led through the pins to the routing areas at the side. Compared to the conditions on an AdvancedTCA backplane, where this number of signals can be distributed over 6U, the challenge for the MicroTCA backplane becomes clear. The same number of signals has to be accommodated in only 1.5U. Accomplishing this without increasing the number of layers, which would make the backplane more expensive, can only be achieved with the advantage of extensive backplane design experience.

For cost-sensitive industrial applications fabric signals can be routed directly between the slots. Many cases require only a few slots, resulting from the density of the AdvancedMC modules. Designers can significantly reduce the number of layers with directly connected slots to achieve very cost-effective solutions.

Despite the different backplane topologies, the user does not have to worry that an AdvancedMC might be damaged by an incompatible fabric interface. The carrier manager on the MCH reads the backplane topology from the chassis FRU data stored in an EEPROM on the backplane, reads the fabric interface information from the FRU data on the AdvancedMCs, and enables only compatible fabric ports.

No explosion of topologies and module widths

The initial fear that many possible topologies and module widths would lead to an enormous number of customer-specific backplanes has not been founded. Most users have concentrated on star or dual star topologies. With respect to AdvancedMCs, the 4 HP width recently added to the specification is now well established. Many modules originally built in a 6 HP width have been redesigned as 4 HP mid-size modules. Compact modules (3 HP width) only play a subordinate role now, and the full-size modules (6 HP) are only used for AdvancedMCs with very large components. Therefore a limited number of backplane configurations can be developed, which can then serve as a starting point for customer-specific applications. Designers can thus adapt the system topology with only minor changes to individual applications.

Figure 1

Free ports and different transfer protocols

The ports on the AdvancedMC module are divided into four regions for different functions: Common Options, Fat Pipe, Extended Fat Pipe, and Extended Options (Figure 2). The storage interface is located in the Common Options area. This interface provides the connections to hard disk drive AdvancedMCs. To construct a storage server, all HDD and CPU AdvancedMC slots can be connected via a Serial ATA or SAS switch on one or both MCHs in star topology. For other applications it is sufficient to connect dedicated CPU AdvancedMC slots on the backplane via direct links with one or two slots for hard disk drive AdvancedMCs. Most data transfer takes place in the Fat Pipe and the Extended Fat Pipe regions. Typically four of the Fat Pipe ports on each AdvancedMC are connected to MCH 1, and four Extended Fat Pipe ports are connected to MCH 2. The Extended Options region is typically used for redundancy. There are still free ports in this region that have not been defined. However, suggestions are available from AdvancedMC module manufacturers and the SCOPE Alliance for how these could be used in future.

In order to use two different transfer protocols in one MicroTCA system you can use two ports for Gigabit Ethernet and two for PCI Express or Serial RapidIO. The newest proposal from the SCOPE Alliance uses the Fat Pipe ports 4 through 7 for PCI Express with point-to-point connections between the AdvancedMC slots. The Extended Fat Pipe ports 8 to 11 would be used for GbE/XAUI or Serial RapidIO but connected to MCH1 instead of MCH2. For redundancy the XAUI and Serial RapidIO lines to MCH2 would be located on the AdvancedMC ports 17 to 20 in the Extended Options region. With that proposal, it will be possible to run XAUI and Serial RapidIO in a redundant mode. It would also be possible to run PCI Express together with XAUI or Serial RapidIO in the same system. The protocol used does not make any difference to the backplane, but the data exchange on the MCH and the connected AdvancedMCs are protocol dependent. Therefore new thoughts in this direction are to use two different protocols and use the AdvancedMC module user-defined ports 12 to 20.

Another issue is providing the correct clock signal for the software protocol. The AMC.0 R.1.0 specification defined CLK1 to CLK3. These clock definitions were imported into the MicroTCA specification. AMC.0 R1.0 defines all three clocks as telecom clocks, with CLK1 and CLK3 as outputs from the MCH to the AdvancedMC, and CLK2 as an input from each AdvancedMC to both MCHs. The fabric clock (FCLK) for PCI Express was not defined. The AMC.0 R.2.0 specification changed the clock definitions. CLK1 and CLK2 were renamed to TCLKA and B (Telecom Clock); CLK3 is now used as the FCLKA. AdvancedMC port 16 is redefined as TCLK C and D. That allows a complete redundancy for the telecom clocks (input and output). In addition a fabric clock is defined. These changes have to be imported into the net revision of the MicroTCA specification.

Due to the different protocols and the corresponding clocks, the user has to be careful to choose the right backplane topology. The most important question is: Which fabric protocols are used between the different AdvancedMCs? Does the user need only a point-to-point connection between dedicated AdvancedMC slots or a star topology? Is redundancy needed? Where is the clock signal generated, and where must it be distributed? A good way to document the required interconnects is to create a topology sheet such as that of Figure 2.

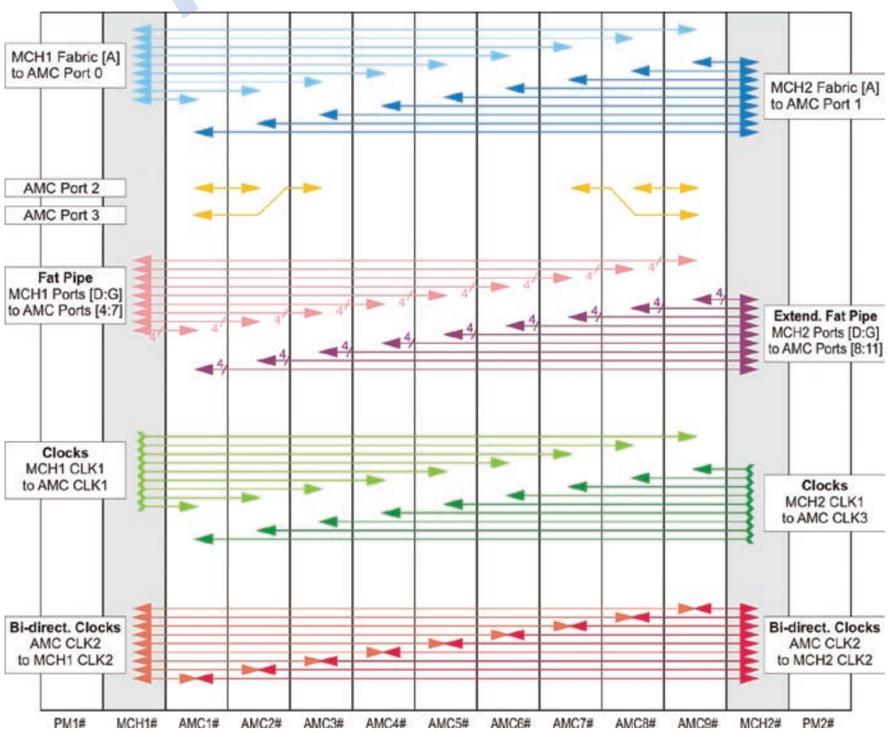

Figure 2

It's time for new design guidelines

Backplanes that can transfer several gigabits per second per port must obey the same laws of physics as their predecessors. Conventional design guidelines that were used for parallel buses such as VMEbus and CompactPCI will fail with high-speed fabrics. With the very high signal speeds losses in the dielectric material and the skin effect play a large role. Even more critical, however, is the configuration of vias, the transfer points of signal lines from one layer to the next, and Plated Through Holes (PTHs), where connectors are pressed into the backplane. These could be ignored with the old "MHz" buses, but are creating problems in MicroTCA backplanes from several viewpoints:

- Stub effect resonances that are generated in the via influence the signal transfer immensely
- The capacitance of the PTH causes a strong impedance discontinuity on which the signal energy is reflected and worsens the signal-to-noise relationship
- The capacitance of the via has the effect of a low-pass filter, which removes the high frequency parts of the signal that are required for the transfer of serial protocols

Backdrilling, a conventional technique to push the resonance frequencies to higher values, the omission of nonfunctional pads in a PTH, and creation of the largest possible antipads are only a few measures that can lead to success. Equally indispensable are simulations made with 3D field solver software before the backplane is designed.

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